

IN THE CLAIMS:

Claim 1 (original) A semiconductor memory device comprising:
a memory cell array including a plurality of blocks, each of the blocks including memory cells arranged in rows and columns;
a block select circuit configured to select one of the blocks of the memory cell array;
a plurality of word-line-driving-signal lines to receive voltages to be applied to a plurality of word lines in each block; and
a plurality of transfer transistors having current paths thereof connected between the word-line-driving-signal lines and the word lines of the each block, the transfer transistors being controlled by outputs from the block select circuit, any two of the transfer transistors, which correspond to each pair of adjacent ones of the word lines, being separate from each other lengthwise and widthwise, one or more transfer transistors corresponding to another word line or other word lines being interposed between the any two transfer transistors.

Claims 2-30 (Cancelled)